8-bit A/D and D/A converter

PCF8591

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I²C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I²C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I²C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I²C bus.

Features

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I²C bus
- Address by 3 hardware address pins
- Sampling rate given by I²C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P: 16-lead DIL; plastic (SOT38).
PCF8591T: 16-lead mini-pack; plastic (SO16L; SOT162A).

8-bit A/D and D/A converter PCF8591

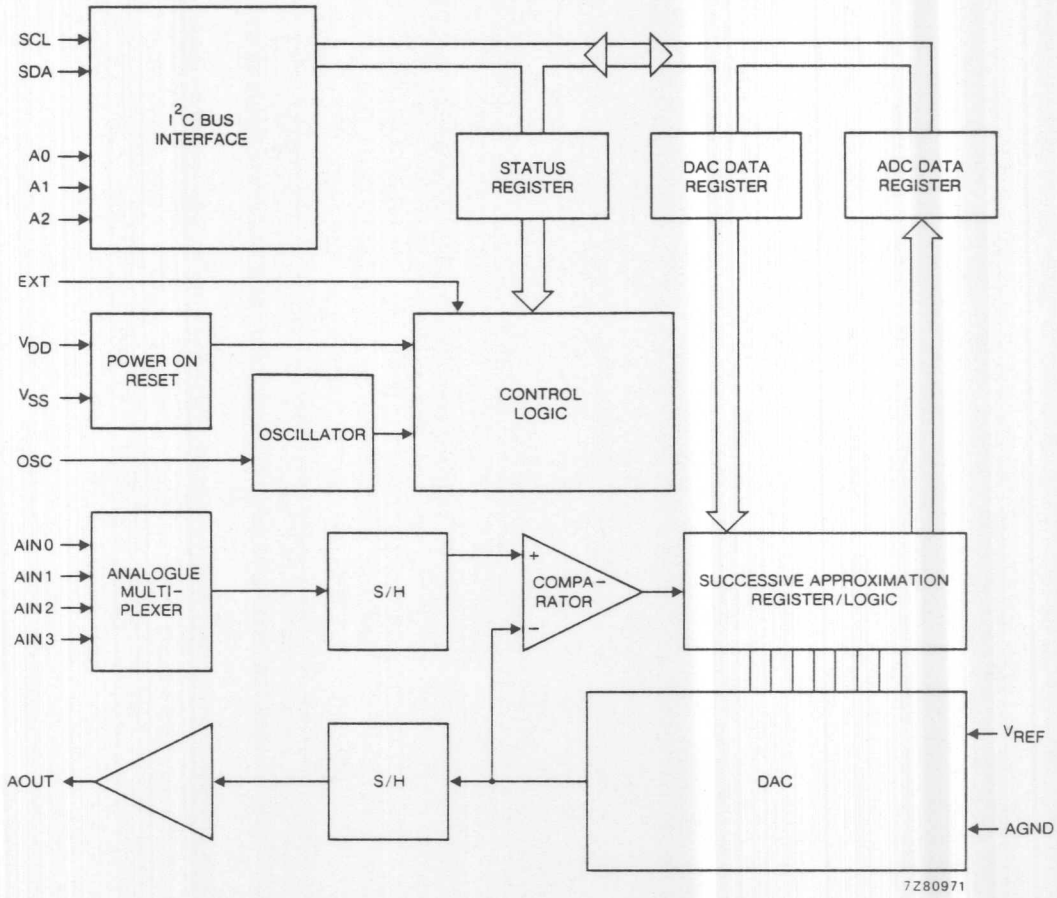

Fig. 1 Block diagram.

8-bit A/D and D/A converter | PCF8591

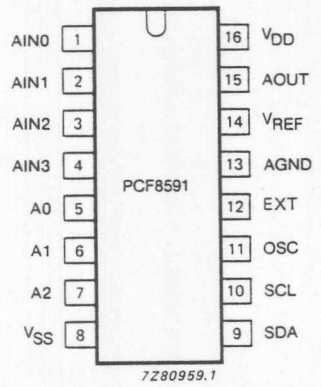

Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I²C bus data input/output
10.	SCL	I²C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Adressing

Each PCF8591 device in an I²C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I²C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3 and 10).

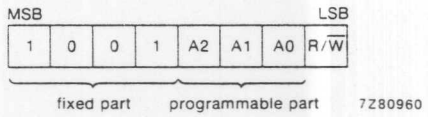

Fig. 3 Address byte.

Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analogue output, and for programming the analogue inputs as single-ended or differential inputs. The lower nibble selects one of the analogue input channels defined by the upper nibble (see Fig. 4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.

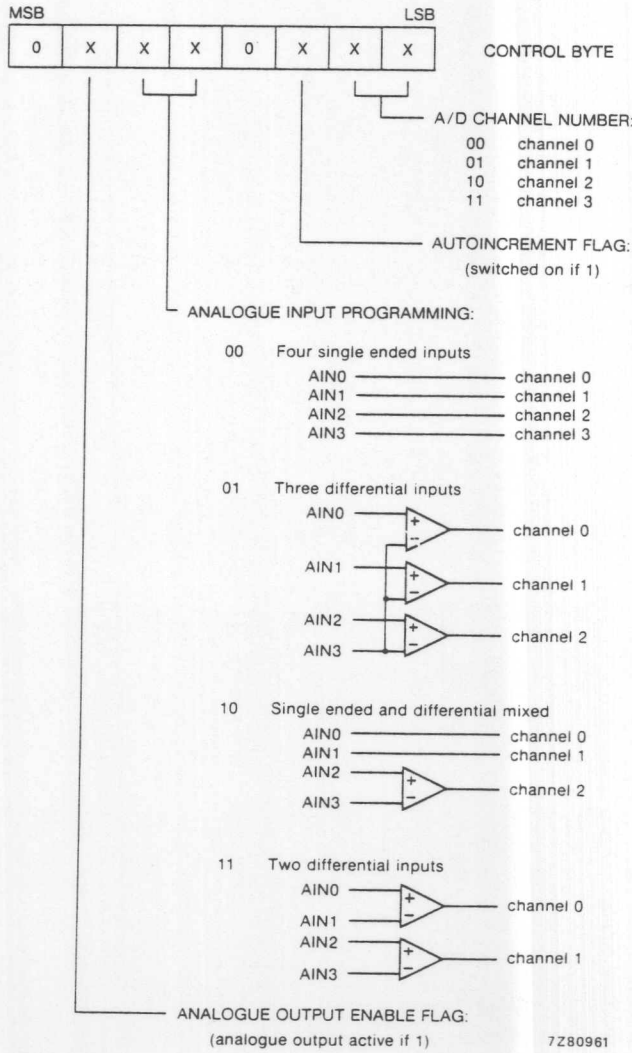

Fig. 4 Control byte.

D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analogue voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6. The waveforms of a D/A conversion sequence are shown in Fig. 7.

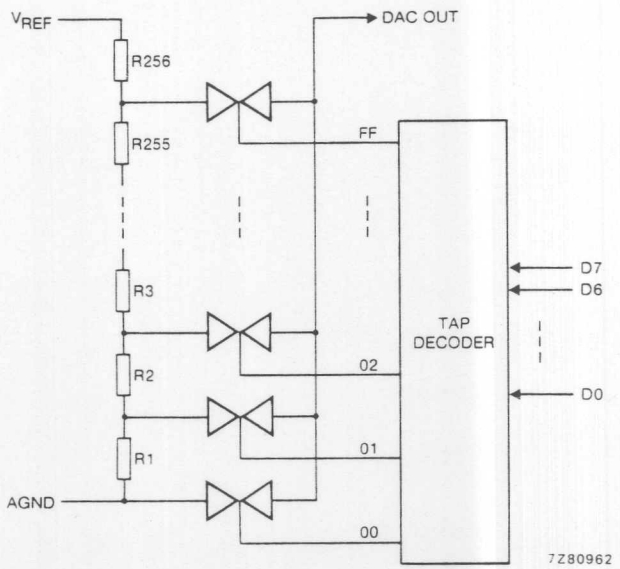

Fig. 5 DAC resistor divider chain.

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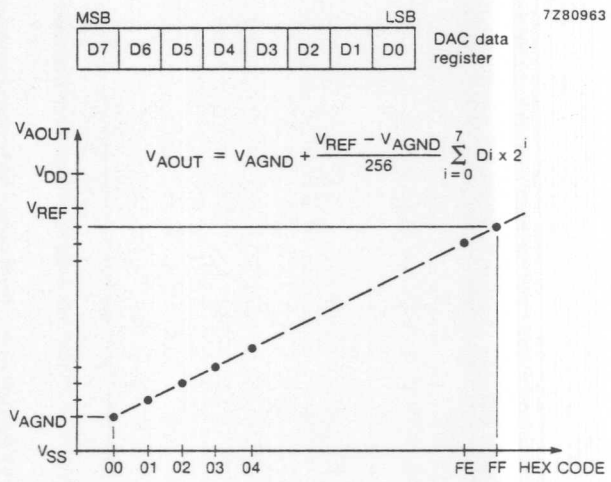


Fig. 6 DAC data and d.c. conversion characteristics.

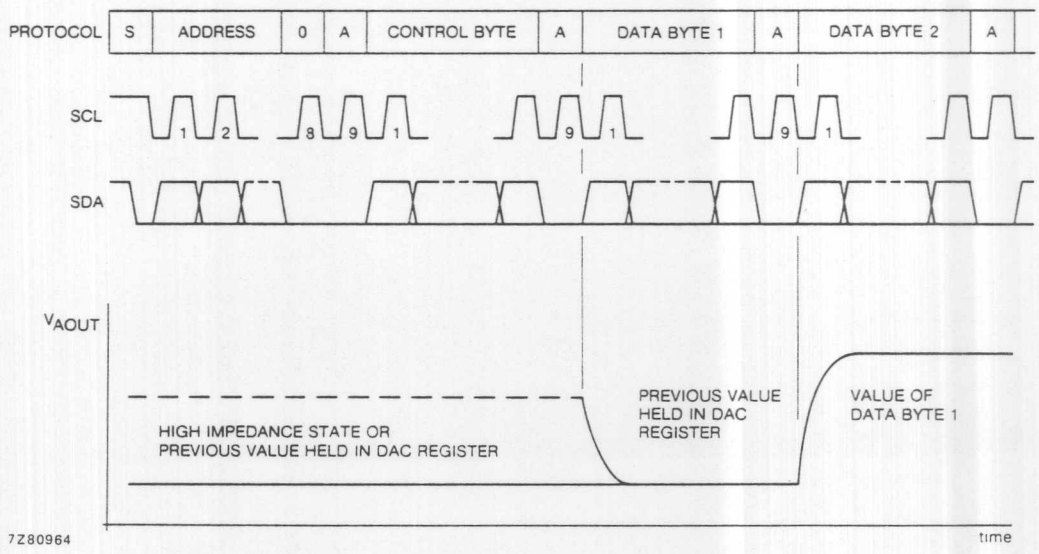


Fig. 7 D/A conversion sequence.

A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig. 8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Fig. 9). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I²C bus read cycle is shown in Fig. 10.

The maximum A/D conversion rate is given by the actual speed of the I²C bus.

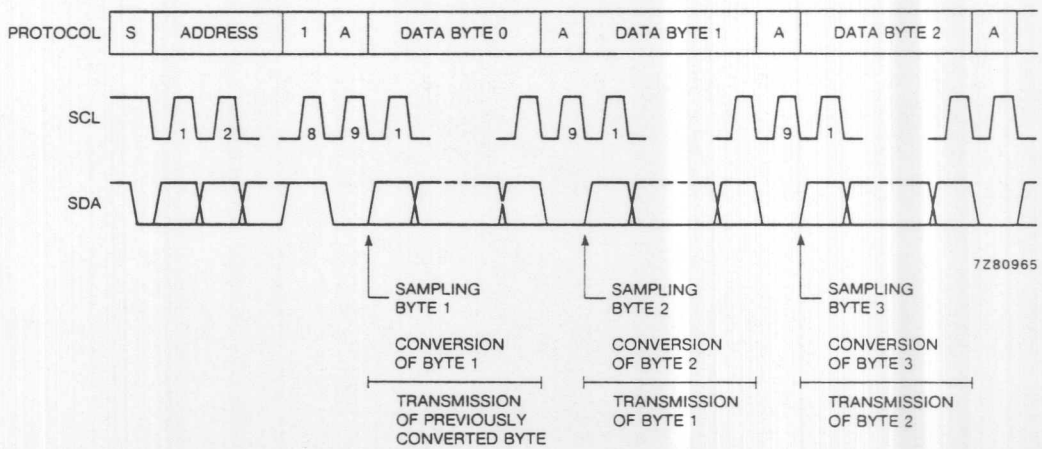


Fig. 8 A/D conversion sequence.

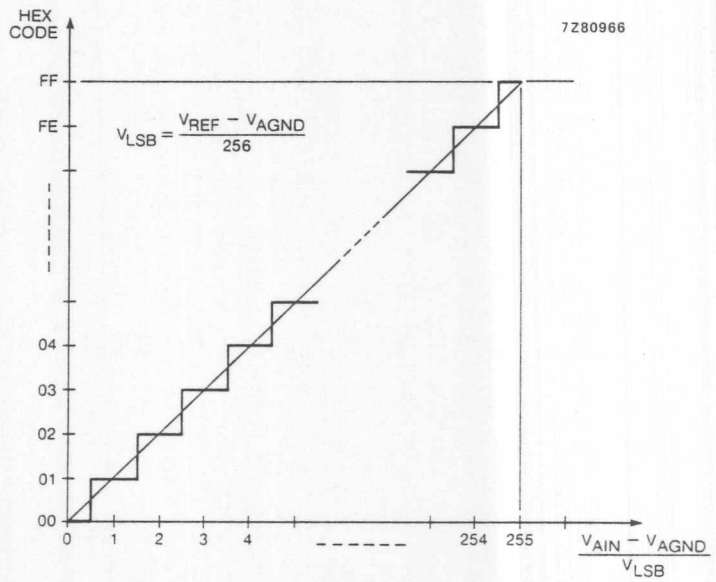


Fig. 9a A/D conversion characteristics of single-ended inputs.

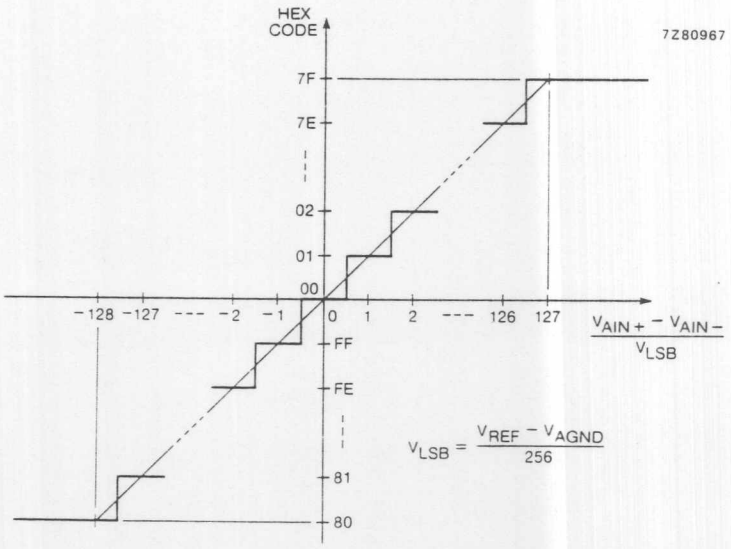


Fig. 9b A/D conversion characteristics of differential inputs.

Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analogue ground and may have a d.c. off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Application Information and Fig. 6.

The A/D converter may also be used as a one or two quadrant analogue divider. The analogue input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high impedance state allowing the user to feed an external clock signal to OSC.

Bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I²C bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

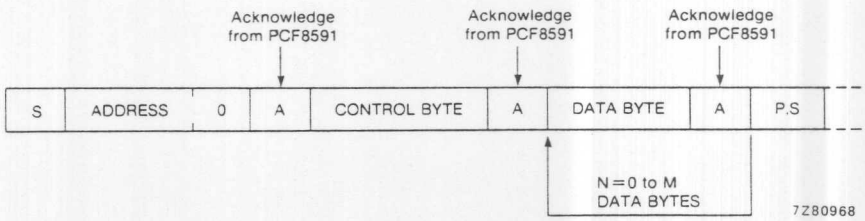


Fig. 10a Bus protocol for write mode, D/A conversion.

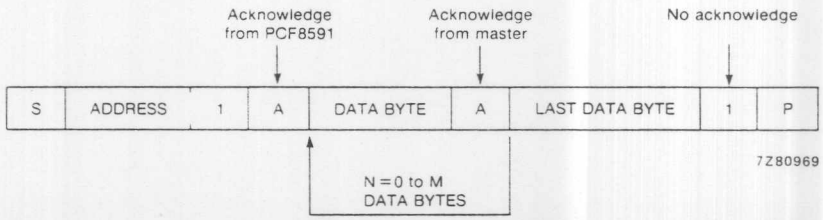


Fig. 10b Bus protocol for read mode, A/D conversion.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transfered during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

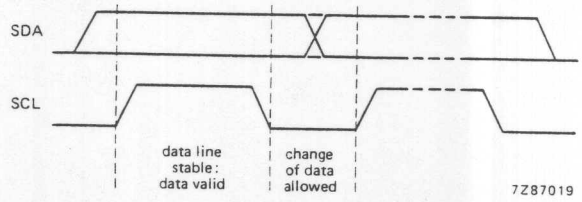


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

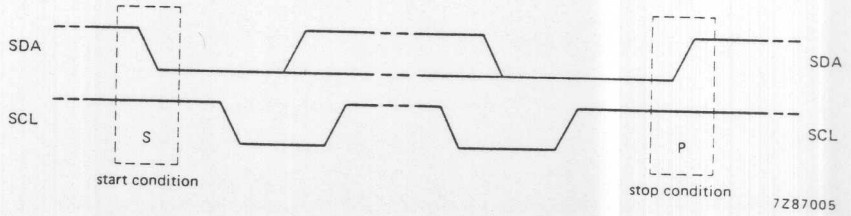


Fig. 12 Definition of start and stop condition.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

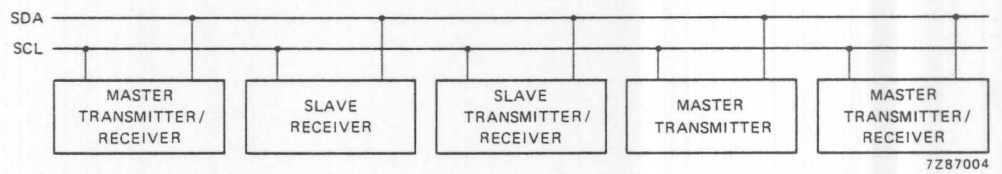


Fig. 13 System configuration.

Acknowledge.

The number of data bytes transfered between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

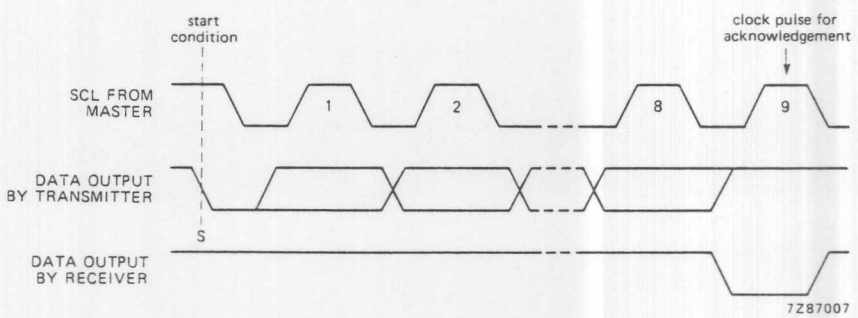


Fig. 14 Acknowledgement on the I²C bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

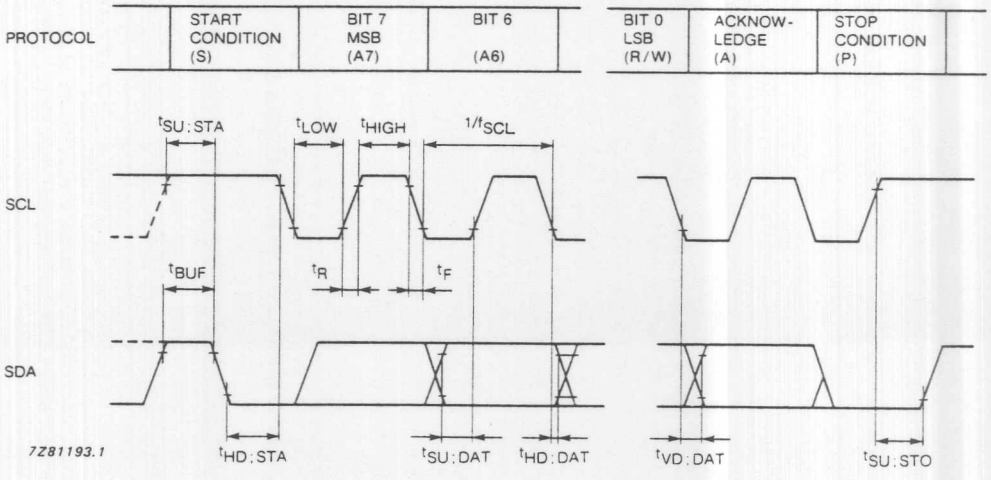


Fig. 15 I²C bus timing diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to +8,0 V
Voltage on any pin	V_I		−0,5 to V_{DD} +0,5 V
Input current d.c.	I_I	max.	10 mA
Output current d.c.	I_O	max.	20 mA
V_{DD} or V_{SS} current	I_{DD}, I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	100 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

Note:

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD}	2,5	–	6,0	V
Supply current	standby V_I = V_{SS} or V_{DD}; no load	I_{DD0}	–	1	15	μA
Supply current	operating; AOUT off; f_{SCL} = 100 kHz	I_{DD1}	–	125	250	μA
Supply current	AOUT active; f_{SCL} = 100 kHz	I_{DD2}	–	0,45	1,0	mA
Power-on reset level	note 1	V_{POR}	0,8	–	2,0	V
Digital inputs/output	SCL, SDA, A0, A1, A2					
Input voltage	LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage	HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input current	leakage; V_I = V_{SS} to V_{DD}	I_I	–	–	250	nA
Input capacitance		C_I	–	–	5	pF
SDA output current	leakage; HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA
SDA output current	LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage inputs						
Voltage range*	$V_{REF} > V_{AGND}$	V_{REF}	$V_{SS}+1,6$	–	V_{DD}	V
Voltage range*	$V_{REF} > V_{AGND}$	V_{AGND}	V_{SS}	–	$V_{DD}-0,8$	V
Input current	leakage	I_I	–	–	250	nA
Input resistance	V_{REF} to AGND	R_{REF}	–	100	–	kΩ
Oscillator	OSC, EXT					
Input current	leakage	I_I	–	–	250	nA
Oscillator frequency		f_{OSC}	0,75	–	1,25	MHz

D/A CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{load} = 10 kΩ; C_{load} = 100 pF; T_{amb} = –40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output						
Output voltage range	no resistive load	V_{OA}	V_{SS}	–	V_{DD}	V
Output voltage range	R_{load} = 10 kΩ	V_{OA}	V_{SS}	–	$0,9 \times V_{DD}$	V
Output current	leakage; AOUT disabled	I_{LO}	–	–	250	nA
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	50	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error	no resistive load	G_e	–	–	1	%
Settling time	to ½ LSB full scale step	t_{DAC}	–	–	90	µs
Conversion rate		f_{DAC}	–	–	11,1	kHz
Supply noise rejection	at f = 100 Hz; V_{DD} = 0,1 V_{PP}	SNRR	–	40	–	dB

* A further extension of the range is possible, if the following conditions are fulfilled:

$$\frac{V_{REF} + V_{AGND}}{2} \geqslant 0,8 \text{ V and } V_{DD} - \frac{V_{REF} + V_{AGND}}{2} \geqslant 0,4 \text{ V.}$$

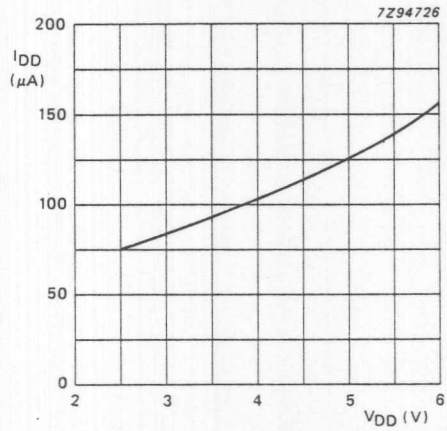
A/D CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{source} = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified

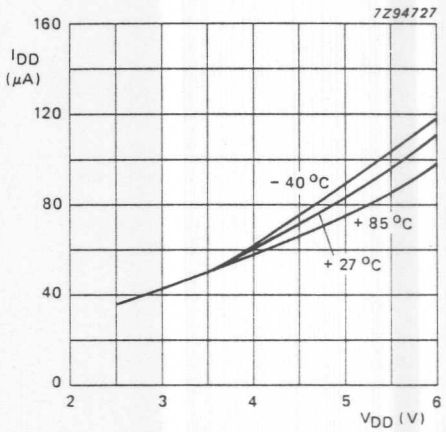
parameter	conditions	symbol	min.	typ.	max.	unit
Analogue inputs						
Input voltage range		V_{IA}	V_{SS}	–	V_{DD}	V
Input current	leakage	I_{IA}	–	–	100	nA
Input capacitance		C_{IA}	–	10	–	pF
Input capacitance	differential	C_{ID}	–	10	–	pF
Single-ended voltage	measuring range	V_{IS}	V_{AGND}	–	V_{REF}	V
Differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	V_{ID}	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	20	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error		G_e	–	–	1	%
Gain error	small-signal; ΔV_{IN} = 16 LSB	GS_e	–	–	5	%
Rejection ratio	common-mode	CMRR	–	60	–	dB
Supply noise rejection	at f = 100 Hz; V_{DDN} = 0,1xV_{PP}	SNRR	–	40	–	dB
Conversion time		t_{ADC}	–	–	90	μs
Sampling/conversion rate		f_{ADC}	–	–	11,1	kHz

Note

1. The power on reset circuit resets the I²C bus logic when V_{DD} is less than V_{POR}.

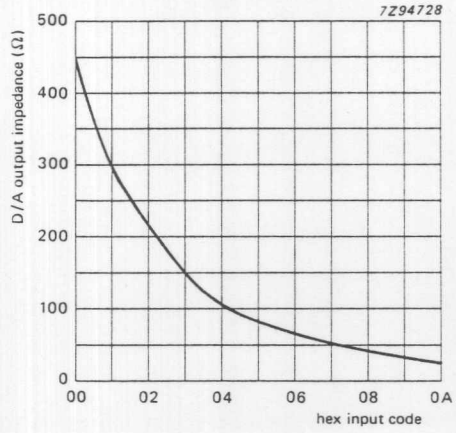


(a) internal oscillator; T_{amb} = + 27 °C.

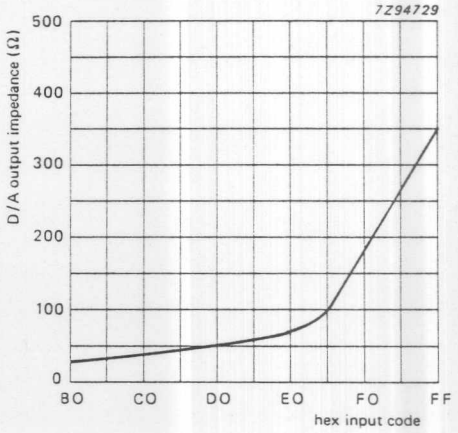


(b) external oscillator.

Fig. 16 Operating supply current against supply voltage (analogue output disabled).



(a) output impedance near negative power rail; T_{amb} = + 27 °C.



(b) output impedance near positive power rail; T_{amb} = + 27 °C.

Fig. 17 Output impedance of analogue output buffer (near power rails).

The x-axis represents the hex input-code equivalent of the output voltage.

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analogue inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analogue signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors (> 10 μF) are recommended for power supply and reference voltage inputs.

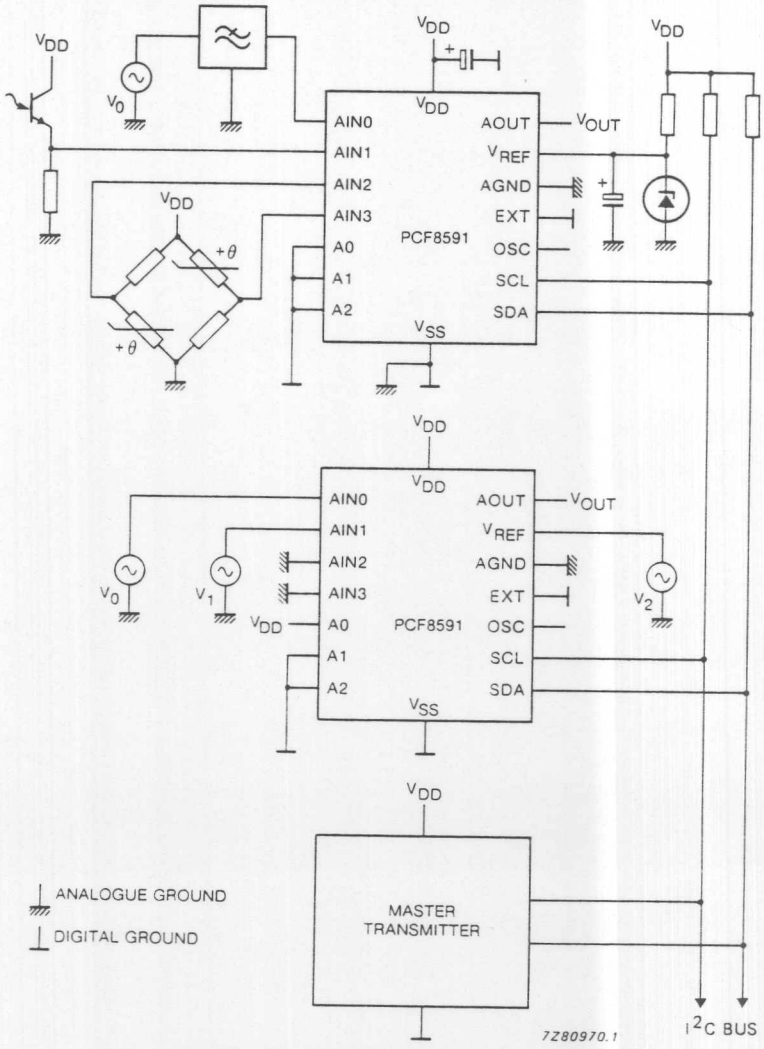


Fig. 18 Application diagram.